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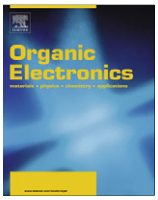

Letter

Leakage current reduction in pentacene-based thin film transistor using asymmetric source/drain electrodes

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ABSTRACT

In this work, we propose the concept of achieving a lower off-current in organic thin film transistors (OTFTs) by asymmetric source/drain with low and high work-function metals. The artificial hole barrier height (h-BH) at the drain-channel junction formed by this method prevents hole carriers transport from source to drain through the pentacene layer during the off-state. On-current is not affected by this artificially formed h-BH because the effective h-BH is reduced in the on-state. As a result, in the asymmetric Ni–Ti and Ni–Al OTFTs, the off-currents are decreased by 12 and 18.3 times, respectively, compared to that in the symmetric S/D device.

1. Introduction

For future flexible display technology, conjugated polymers or small molecules are very attractive materials because of their mechanical flexibility, low fabrication cost, low process temperature, and large area production capability [1,2]. However, the performance of the recent organic thin-film transistors (OTFTs) fabricated on polymers or molecules is unsatisfactory for use in organic light-emitting diode (OLED) panels, organic memory devices, and organic logic circuits because of their low mobility. For this reason, in the aspect of carrier injection rate, detailed studies relating to metal–organic (M–O) junctions for source/drain (S/D) have been sought to increase the on-current and carrier mobility in OTFTs as much as possible [3,4]. Although high Schottky injection barrier exists at the M–O junction interface regardless to the metal work-function due to Fermi level pinning [3], a high carrier injection rate was successfully achieved at the source-channel junction of OTFTs by using (i) graphene electrodes which provide a lower hole barrier height (h-BH) than Au S/D [4] and (ii) Si_3N_4 insertion layer which de-pins the Fermi level [3]. However, this high carrier injection rate by lowering the h-BH also increases the current flowing from source to drain (I_{SD}) in the off-state ($V_{GS} = 0$ V). To date, most of efforts to reduce the off-current in OTFTs are limited to the current flowing between the gate and S/D through the dielectric layer [5,6].

Therefore, in this study, we propose a method to suppress off-current flowing from source to drain through pentacene by making an artificial h-BH at the drain-channel junction. This h-BH at the drain-channel junction is achieved by the concept of asymmetric S/D electrodes using low and high work-function metals for the drain and source, respectively. This artificial h-BH blocks the transportation of hole carriers in the off-state, but it is easily tunneled in on-state ($V_{GS} = -60$ to -80 V), providing sufficiently high on-current by high electric field at the drain-channel junction.

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2. Experiments

Approximately 160 and 30 nm thick pentacene layers were thermally evaporated at below 10^{-5} Torr on (i) (1 0 0) *p*-type Si substrates (0.007–0.02 Ω cm) to fabricate vertical M–O junction diodes and (ii) on 300 nm thick SiO_2/(1 0 0) *n*-type Si substrates (0.007–0.02 Ω cm) to make OTFTs, respectively. For the M–O junction diodes, 25 nm thick contact metal (Ni, Ti, or Al) and 200 nm thick Al metal pad layers were deposited on 160 nm thick pentacene films in a thermal evaporation system with a shadow mask. In the same way, we then prepared three different transistor samples with symmetric (Ni at source/Ni at drain) and asymmetric (Ni at source/Ti or Al at drain) S/D electrodes on the pentacene/SiO_2/*n*-Si substrates. In particular, we extracted contact resistance (R_c) at different gate biases ($V_G = 0$, -10, and -20 V) in the two selected junctions, Ni–pentacene (with the lowest h-BH) and Al–pentacene (with the highest h-BH) junctions, by transfer length method (TLM). The TLM structure consists of an electrode area of 100 × 200 μm and contact distances of 100, 120, 160, 240, 320, and 420 μm. Finally, we measured and analyzed current–voltage (*I*–*V*) characteristics of the M–O junction diodes and the symmetric/asymmetric S/D OTFTs. For these OTFTs, as-deposited pentacene film was used although the (0 0 1) pentacene peak appeared after annealing the pentacene film at 50, 100, and 150 °C. This is because the root mean square (RMS) surface roughness and resistivity values were respectively decreased and increased as a function of the post-deposition annealing temperature.

3. Results and discussion

Fig. 1(a) shows the *I*–*V* characteristics of the M–O junction diodes formed on the pentacene layer with Ni, Ti, and Al contact metals. The forward currents of the Ti- and Al–pentacene junction diodes increase more slowly as a function of the applied junction bias (V_A) compared to the Ni-pentacene one, because of their h-BHs (=$qV_{bi,Ti}$ and $qV_{bi,Al}$ in the equilibrium state) shown in Fig. 1(b). The h-BHs seem to prevent the hole carriers from being transported from pentacene to Ti and Al under low forward bias (negative voltage). However, these forward currents become comparable to that of the Ni–pentacene junction diode at forward bias around -2 V, because the initial h-BHs decrease and disappear eventually as V_A continually increases. This can be easily understood according to the relationship between h-BHs and V_A, where h-BHs = $q(V_{bi,Ti} - V_A)$ and $q(V_{bi,Al} - V_A)$. In contrast, the BH (=$qV_{bi,Ni}$ in the equilibrium state) in the Ni–pentacene junction does not prevent the hole carriers from being transported, because the Fermi level of Ni ($E_{F,Ni}$) is still located closer to the highest occupied molecular orbital (HOMO) band of pentacene, even though it is pinned irrespective of the metal work-function [3,7]. In addition, a very high reverse current (positive voltage) was observed in the Ni–pentacene junction diode, because of its very low h-BH, which is known as being about 0.6 eV [5]. However, in the Ti– and Al–pentacene junction diodes, the reverse currents were dramatically suppressed by the increased h-BHs (∼1.5 eV) [7]. It should be noted that Ti and Al still possess much higher h-BH than Ni on the pentacene film, even though it is already known that h-BH is varied due to (i) the oxidation of the metal and (ii) its penetration into the pentacene film [8].

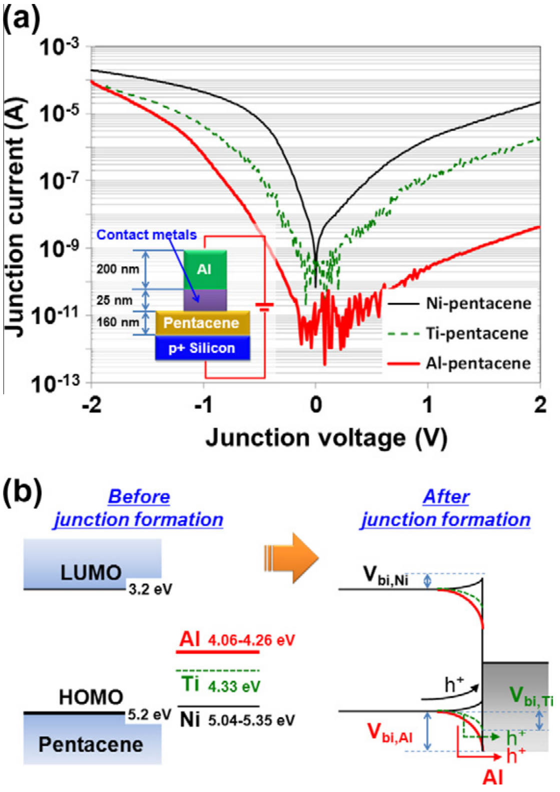

Fig. 1. (a) *I*–*V* characteristics of Ni-, Ti-, and Al–pentacene junction diodes. (b) Schematic energy band diagrams of the Ni-, Ti-, and Al–pentacene junctions in the equilibrium state.

The BH difference of the metal–pentacene junctions was also confirmed by the R_c data extracted by TLM with the Ni and Al electrodes, representing the lowest and highest work-function contact metals, respectively (Fig. 2). Fig. 2(a) shows the linear dependence of the total resistance (R_t) measured in the Ni–pentacene TLM structure on the channel length. Here, the R_t values obtained from the I_D–V_D curves at different gate biases ($V_G = 0$, -10, and -20 V) were plotted. R_c was obtained by finding the *y*-intercept of the extrapolating fit of R_t versus length data, and was plotted as a function of V_G in Fig. 2(b) along with R_c that was extracted from the Al–pentacene TLM structure in the same manner. In all cases, the R_c value of the Al–pentacene junction was around 100 times higher than that of the Ni–pentacene junction. According to the relationship between R_c and BH below, we predict that the Al–pentacene junction always has a higher h-BH even if the OTFT is in the operating condition.

$$R_c = \frac{k}{qA^*T} \exp\left(\frac{q\Phi_{H,eff}}{kT}\right)$$

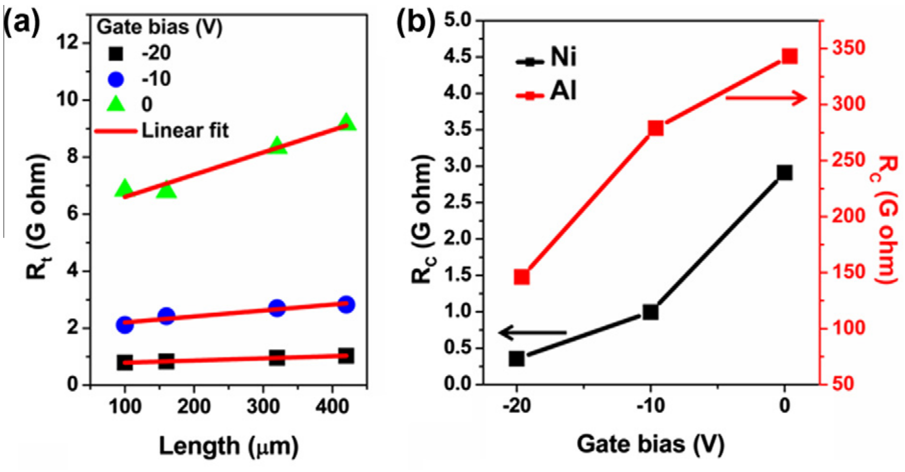

Fig. 2. (a) Linear dependence of the total resistance (R_t) of the Ni–pentacene TLM sample on the channel length at the different gate biases (V_G = 0, −10, and −20 V). (b) Contact resistance (R_c) measured in the Ni- and Al–pentacene TLM samples as a function of V_G.

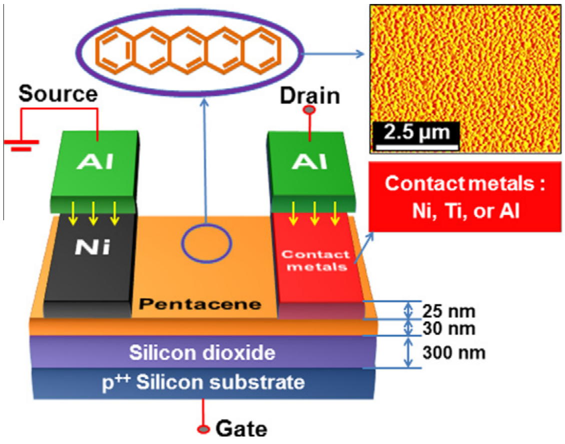

Fig. 3. A schematic diagram of the fabricated symmetric (Ni–Ni) and asymmetric (Ni–Ti and Ni–Al) OTFTs and an AFM image of the deposited pentacene film.

The reduction of R_c as V_G increases is because the higher electric field applied in the metal–pentacene junction increases the BH lowering effect ($\Delta\Phi_H$) and consequently reduces the effective h-BH ($\Phi_{H,eff}$).

$$\Phi_{H,eff} = \Phi_H - \Delta\Phi_H \text{ and } \Delta\Phi_H = \sqrt{\frac{qE}{4\pi\varepsilon}}$$

where $\Phi_{H,eff}$ and Φ_H respectively indicate effective and ideal where $\Phi_{H,eff}$ and Φ_H respectively indicate effective and ideal hole barrier heights, q is electronic charge, E is electric field, and ε is permittivity of pentacene.

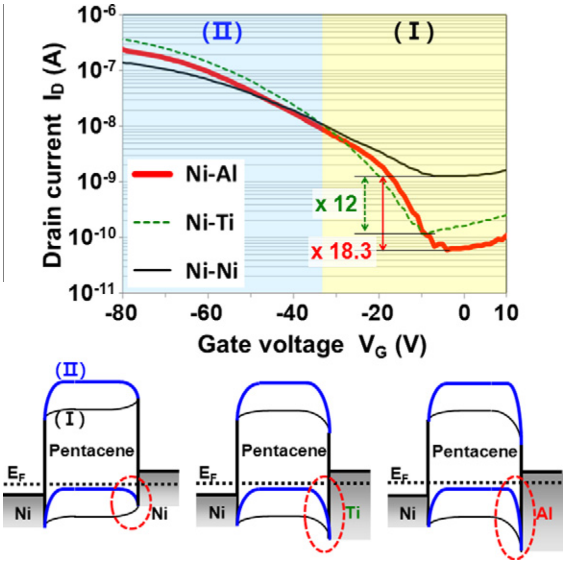

Fig. 4. I_D–V_G characteristics of the symmetric (Ni–Ni) and asymmetric (Ni–Ti and Ni–Al) OTFTs, and schematic energy band diagrams of the OTFTs in the two gate bias regions (I and II).

Fig. 3 shows a schematic diagram of the fabricated symmetric and asymmetric OTFTs. In the fabricated asymmetric S/D OTFTs as shown in Fig. 4, the off-current was decreased by 12 times in the Ni–Ti OTFT and 18.3 times in the Ni–Al OTFT compared to the symmetric S/D device. Since thick thermal SiO_2 layer of 300 nm was used for the gate dielectric in the OTFTs, most of the off-current was attributed to the I_{SD} flowing through the pentacene film. This off-current was suppressed by making an artificial h-BH at the drain-channel junction. As seen in Fig. 1(b), in the equilibrium state, $V_{bi,Ti}$ and $V_{bi,Al}$ act as h-BH blocking hole carriers which transport from pentacene to metal. As a result, lower off-currents were obtained in the asymmetric S/D devices compared to the symmetric S/D device. As V_G increases negatively, holes are accumulated in the channel region and the pentacene channel layer becomes more *p*-type (Bias region II in Fig. 4). Even though the h-BH of the Al- and Ti–pentacene drain-side junctions keeps increasing in region II, their effective h-BH is reduced due to the increased electric field and consequently causes higher tunneling probability. In the asymmetric S/D devices, therefore, the hole carrier transport are not suppressed by the h-BH on the drain-side anymore and, consequently, we obtained on-currents comparable to that of the symmetric S/D device. At the bias condition where $V_G = -80$ V and $V_D = -50$ V, the mobility values extracted from the asymmetric S/D devices (Ni–Ti: 1.7×10^{-3} cm^2/V s and Ni–Al: 10^{-3} cm^2/V s) were slightly higher than that of the symmetric S/D device (Ni–Ni: 5.3×10^{-4} cm^2/V s). Since the poor crystal quality of the pentacene films in this study results in a low accumulation carrier mobility, the improvement of their crystal quality is necessary for better mobility. However, we predict that the asymmetric S/D off-current reduction method will be still valid regardless of the crystal quality of the pentacene films, because the relative work-function difference among metals, such as Ni, Ti, and Al is similar for different quality pentacene films [7,9]. In addition, owing to the decreased off-current, higher on/off current ratio (Ni–Ti: 3.6×10^3 and Ni–Al: 3.2×10^3) was achieved in the asymmetric S/D devices. These relatively low current on/off ratio were attributed to the poor crystal quality of the pentacene films and excessively high interfacial trap density between the pentacene and gate dielectric layers. Finally, the threshold voltages of the asymmetric S/D devices were decreased (Ni–Ti: −19.2 V and Ni–Al: −16.1 V) compared to that (Ni–Ni: −12.4 V) of the symmetric device, because of the artificially formed h-BH at the Ti–pentacene and Al–pentacene drain-side junctions.

4. Conclusion

In conclusion, we achieved a low off-current and high on/off current ratio in pentacene-based OTFTs by making used of the concept of asymmetric S/D. The artificial h-BHs at the drain-channel junctions suppressed the transportation of hole carriers in the off-state and, consequently, reduced the off-current by 12 times in the Ni–Ti OTFT and 18.3 times in the Ni–Al OTFT. In addition, since the artificial h-BHs were not effective, due to the tunneling mechanism in the on-state (high V_G), a high on-current was obtained comparable to that of the symmetric S/D device. This asymmetric S/D off-current reduction method is expected to improve the performance of OTFTs for OLED panels, organic memory devices, and organic logic circuits.

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